Listing of Claims

The following listing of claims will replace all prior versions and listings of claims in this application:

1 - 60. (Canceled)

61. (Previously Presented) A non-volatile memory circuit, comprising:

a plurality of memory cells, each memory cell comprising a ferroelectric capacitor connected in series with an access transistor, said plurality of memory cells being connected between a plurality of respective drive lines and a common bit line;

a plurality of word lines connected respectively to control terminals of said access transistors for activating respective ones of said access transistors in response to a selection signal for selecting one of said memory cells; and

a differential sense amplifier for reading from and writing to said memory cells, said sense amplifier having a first input connected to said bit line, and a second input connected to receive a reference signal, said sense amplifier having a data input terminal and a data output terminal, said sense amplifier for differentially comparing signals on said first and second input lines for reading a data state from a selected one of said memory cells, and for applying a data state read from said selected memory cell to said data output terminal, and said sense amplifier for driving said bit line connected to said selected memory cell to one of a set of predetermined voltage states corresponding to a data state received at said data input terminal for writing said received data state into the selected one of said memory cells.

62. (Previously Presented) A non-volatile memory circuit as recited in claim 61 wherein said reference signal is a predetermined voltage.

63. (Canceled)

64. (Previously Presented) A non-volatile memory circuit as recited in claim 61 including multiple sets of said memory cells, each set having a respective common bit line

thereby forming a memory circuit matrix comprising rows and columns of said memory cells.

65. (Previously Presented) A non-volatile memory circuit as recited in claim 61 including means for isolating said sense amplifier from said bit line.

66. (Canceled)

67. (Previously Presented) A non-volatile memory circuit, comprising:

a plurality of memory cells each including a ferroelectric capacitor connected in series with an access transistor, said plurality of memory cells being connected between a plurality of respective bit lines and a common drive line,

a word line connected to control terminals of said access transistors for activating said transistors in response to a selection signal for selecting one of said memory cells, and

a plurality of differential sense amplifiers corresponding respectively to said bit lines for reading from and writing to memory cells associated with the bit lines, each sense amplifier having a first input connected to the corresponding bit line and a second input connected to receive a reference signal, each sense amplifier having a data input/output terminal, said sense amplifiers for differentially comparing signals on said first and second inputs thereof for reading a data state from the one of said memory cells connected thereto, and for applying a data state read from said selected memory cell to said output terminal, and said sense amplifiers for driving the corresponding bit lines connected to said memory cells to predetermined voltage states corresponding to a data state received at said input terminal for writing said received data state into the corresponding one of said memory cells.

68. (Previously Presented) A non-volatile memory circuit as recited in claim 67 wherein said reference signal is a predetermined voltage.

69. (Canceled)

70. (Previously Presented) A non-volatile memory circuit as recited in claim 67 including multiple sets of said memory cells, each set having a respective common drive line thereby forming a memory circuit matrix comprising rows and columns of said memory cells.

71. (Previously Presented) A non-volatile memory circuit as recited in claim 67 including respective means for isolating said sense amplifier from the corresponding bit lines.

72. (Previously Presented) In a nonvolatile ferroelectric memory of the type having a plurality memory cells, a bit line coupled to each said memory cell, each said memory cell comprising a ferroelectric capacitor having first and second plate electrodes, the polarization of said capacitors corresponding to the data stored therewithin, the improvement wherein:

said memory further comprising a plurality of word lines and a plurality of plate lines distinct from said bit lines and word lines, each of the memory cells being coupled to a word line, each memory cell being coupled also to a plate line, each plate line being coupled to a capacitor plate electrode of a cell, and

each said memory cell further including a respective switching device located within the memory cell, said first plate electrode of said capacitor in said cell being coupled to one said bit line via said switching device, said switching device being coupled to be controlled by one said word line, said second plate electrode of said capacitor in said cell being coupled to one said plate line.

73. (Previously Presented) In a nonvolatile ferroelectric memory of the type having a plurality of memory cells arranged in rows and columns, each column comprising a bit line coupled to memory cells along the column, each said memory cell comprising a ferroelectric capacitor having first and second plate electrodes, the polarization of said capacitors corresponding to the data stored therewithin, the improvement wherein:

said memory further comprises a plurality of word lines and a plurality of plate liens distinct from said bit lines and word lines, each of the memory cells along a row being coupled to a word line corresponding to the row, each memory cell being coupled also to a

corresponding plate line, each plate line being coupled to plate electrodes in a plurality of said cells.

each said memory cell further including a respective switching device located within the memory cell, said first plate electrode of said capacitor in said cell being coupled to its corresponding bit line via said switching device, said switching device being coupled to be controlled by said corresponding word line, said second plate electrode of said capacitor in said cell being coupled to said corresponding plate line.

74. (Previously Presented) A non-volatile ferroelectric memory comprising as array of memory cells arranged in rows and columns, each said row corresponding to a respective word line, each said column corresponding to a respective bit line,

a respective sense amplifier coupled to each said bit line;

each memory cell comprising a ferroelectric capacitor having first and second plate electrodes and a transistor located within said cell for coupling said first electrode of said ferroelectric capacitor to the corresponding said bit line;

said word line being coupled to a control electrode of said transistor; and

a plate line coupled to the second plate electrode of said ferroelectric capacitor, said plate line being coupled to second plate electrodes of a plurality of capacitors in said array, said plate line being distinct from said word lines and said bit lines.